

NEVER STOP

IMPROVING THE FUTURE



TORU FUJIMORI

2021. 10. 29

FUJIFILM Corporation

Electronic Materials Research Laboratories

Electronic Materials Business Division



**NEVER
STOP**
THANKING YOU FOR YOUR SERVICE
FUJIFILM
Value from Innovation



Fujifilm would like to express its support and gratitude to all the medical staff and volunteers on the front line in the fight against this new invisible, but not invincible enemy.

**COVID-19
PANDEMIC**

Negative-tone imaging (NTI) process for ArF immersion and EUV lithography to improve 'Chemical Stochastic'

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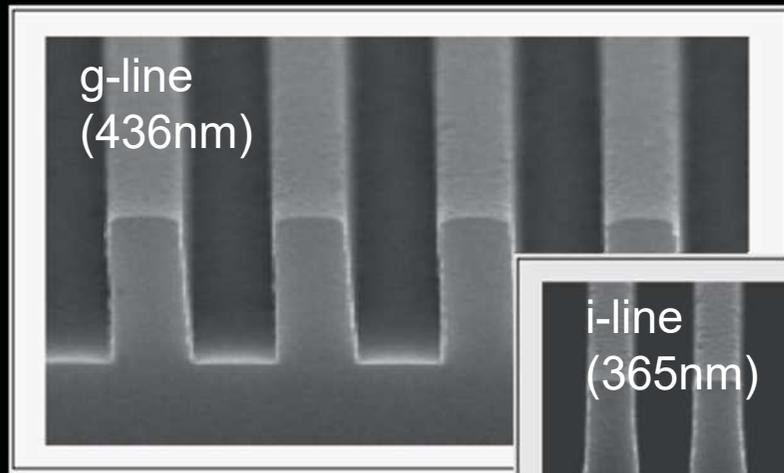
Electronic Materials Research Laboratories

Electronic Materials Business Division

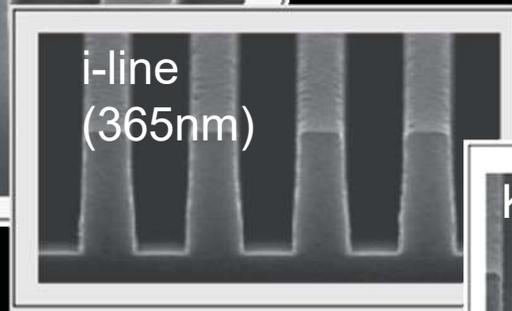


The Pattern shrinkage history

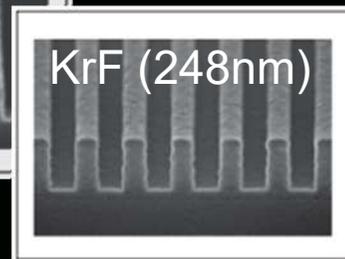
Pattern shrinkage has been driven by shorter exposure wavelength.



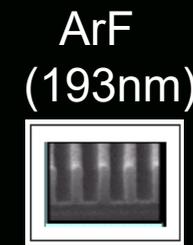
CD = 500nm



350 nm



150 nm



90nm



40nm



15nm

$$\text{Resolution Limit} = k1 \times \frac{\lambda}{NA}$$

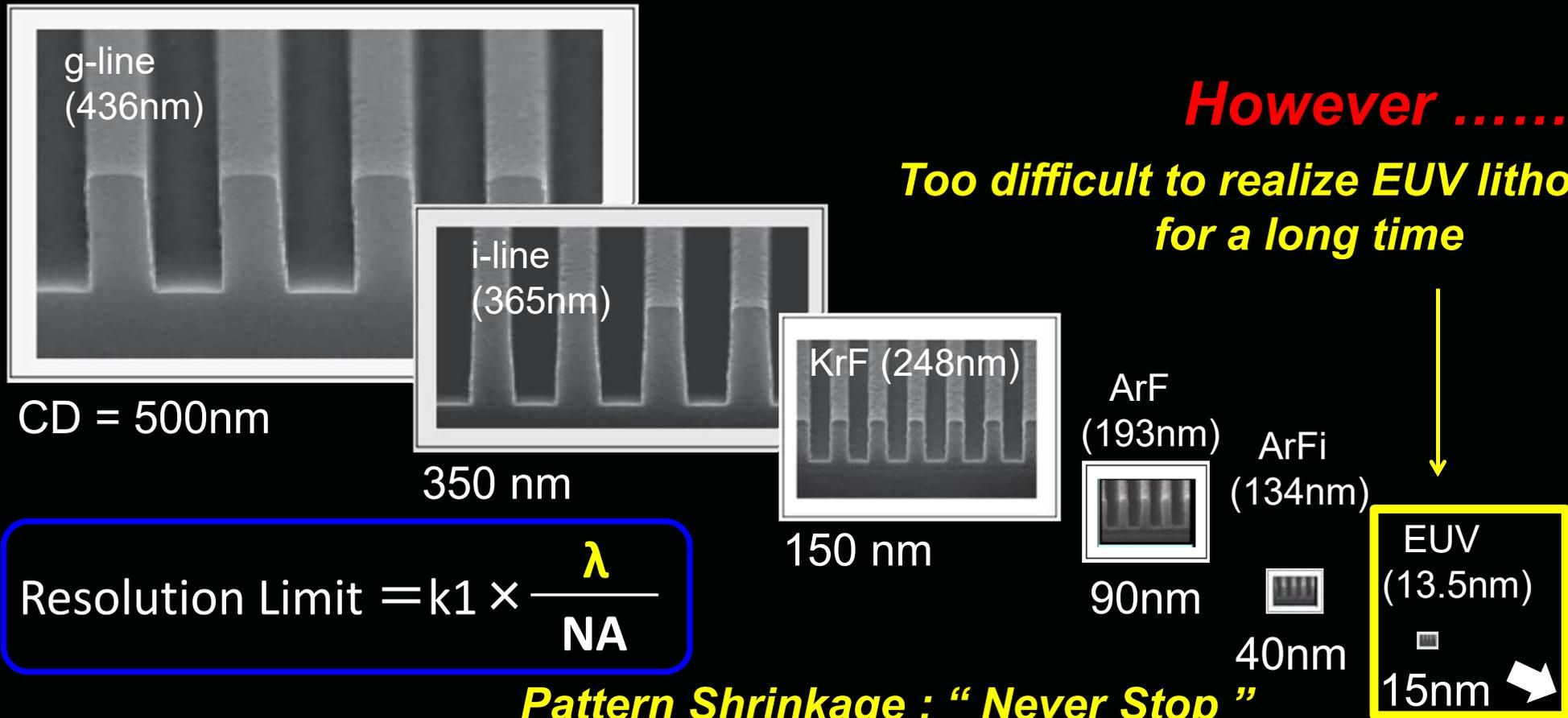
Pattern Shrinkage : " Never Stop "

Resist materials development : " Never Stop "



The Pattern shrinkage history

Pattern shrinkage has been driven by shorter exposure wavelength.



Pattern Shrinkage : “ Never Stop ”
Resist materials development : “ Never Stop ”



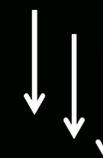
The history of EUV lithography

The first paper of EUV lithography - by Prof. Kinoshita -



Anthony Yen, *EUV lithography: From the very Beginning to the eve of manufacturing (SPIE 2016)*

National Project in Japan



1996

Selete

2011

EIDEC

2019

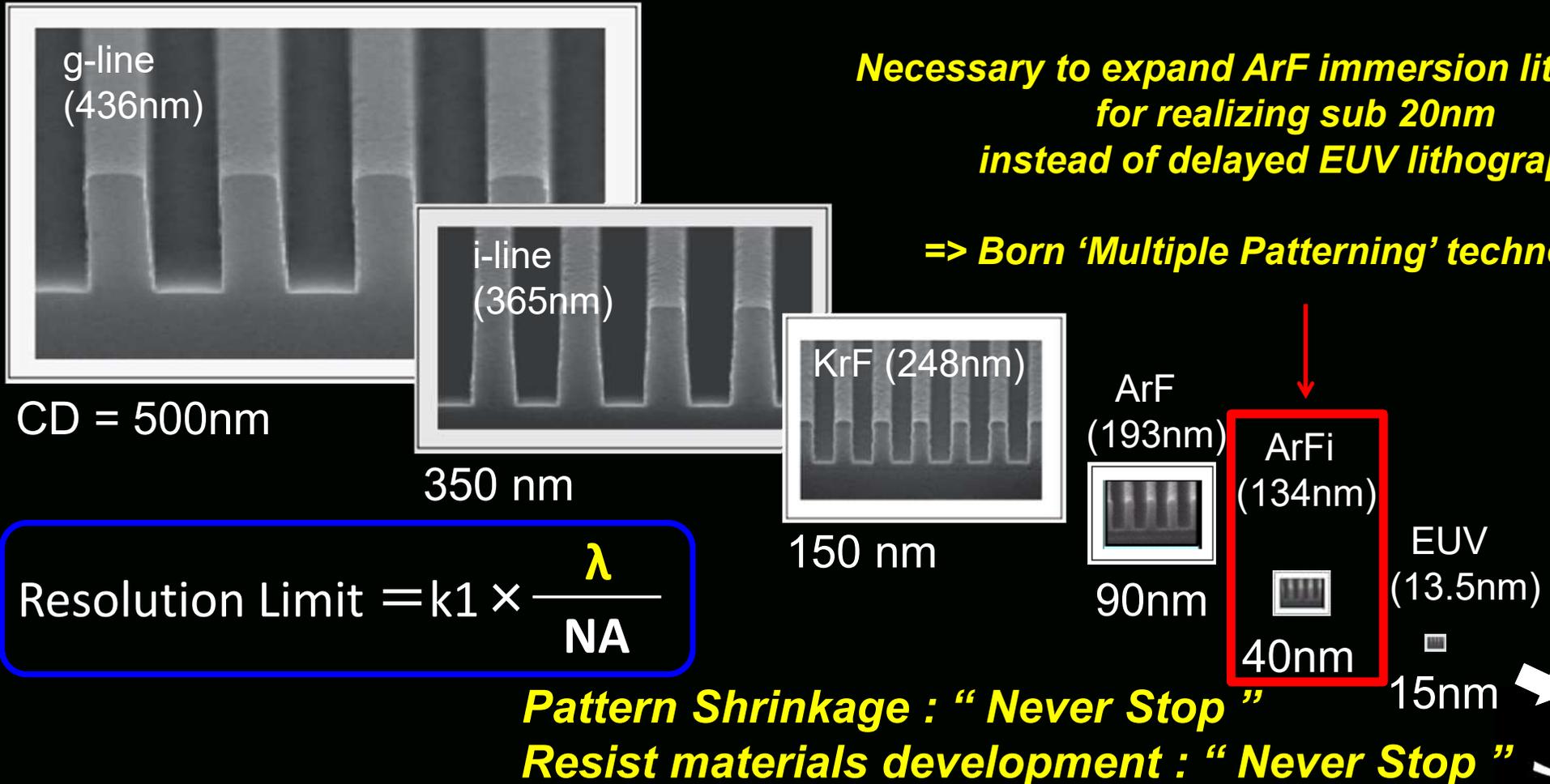
Waiting for EUV lithography for a long time.

Resist materials development : “ Never Stop ”



The Pattern shrinkage history

Pattern shrinkage has been driven by shorter exposure wavelength.

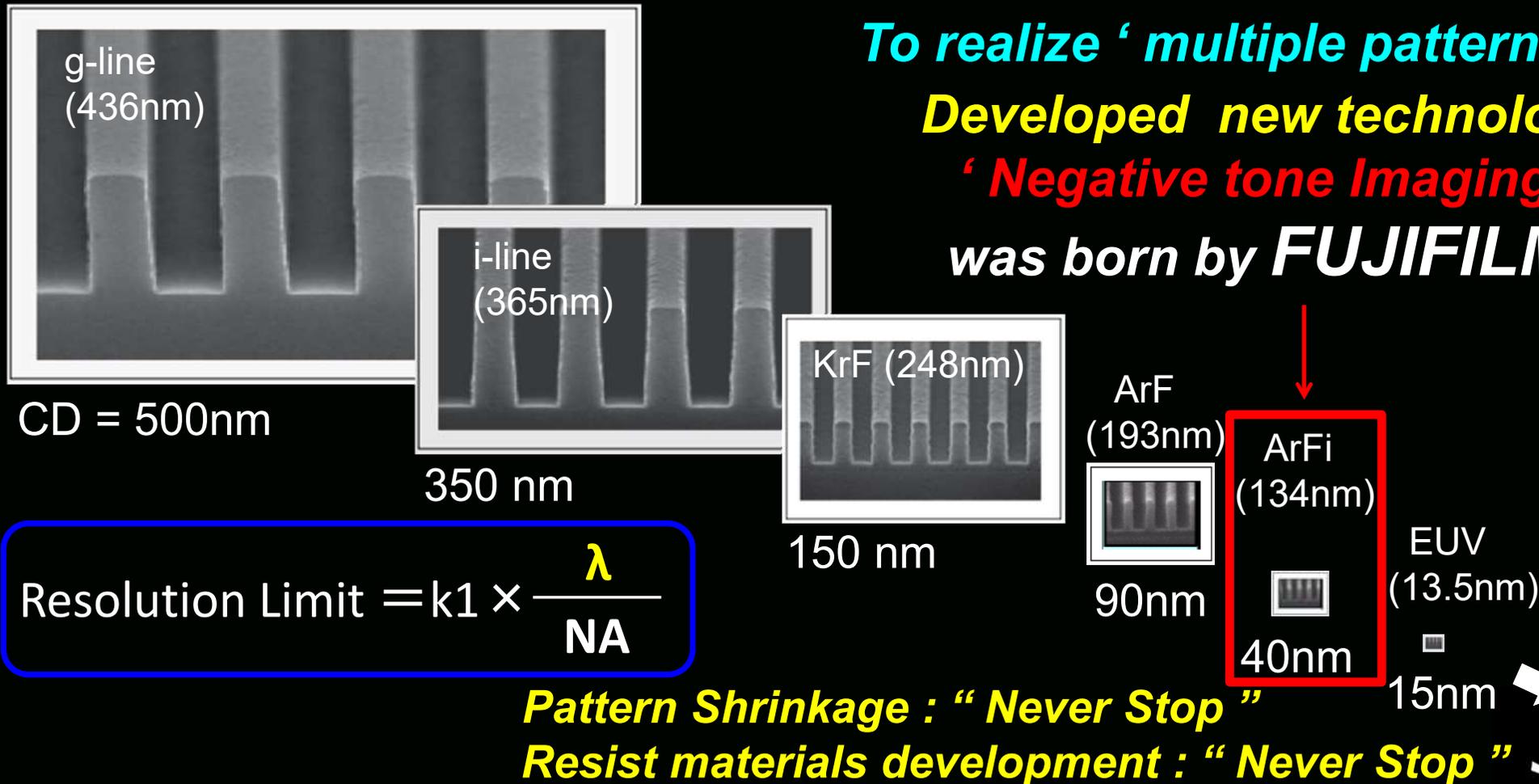


Necessary to expand ArF immersion lithography for realizing sub 20nm instead of delayed EUV lithography

=> Born ‘Multiple Patterning’ technology

The Pattern shrinkage history

Pattern shrinkage has been driven by shorter exposure wavelength.



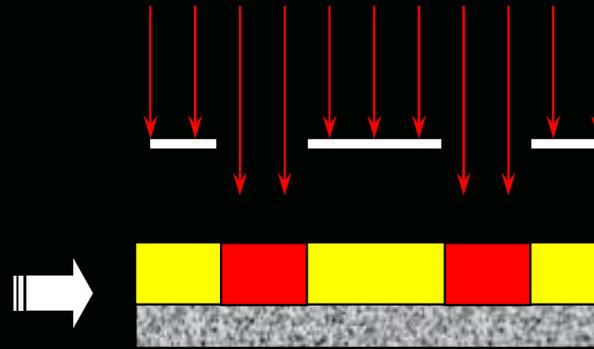
The process flow of the lithography

Key point : Developer (Alkali aqueous based or Organic solvent based)

Resist coating



Exposure & Bake



Development

TMAH aq.



PTI (Positive Tone Imaging)

Organic Solvent

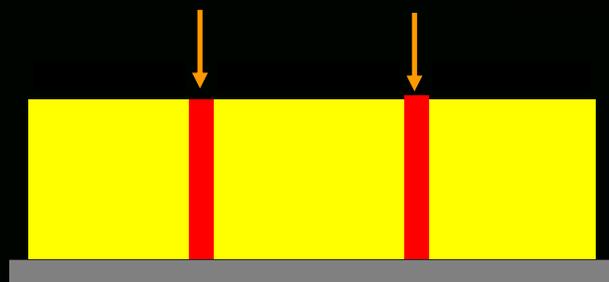


NTI (Negative Tone Imaging)

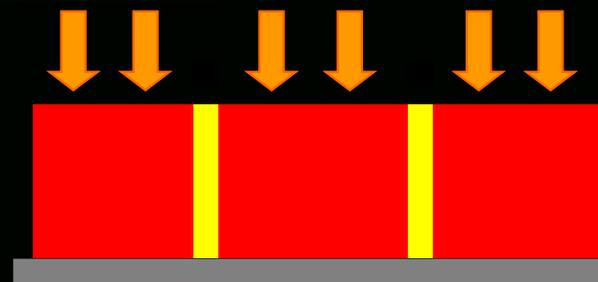
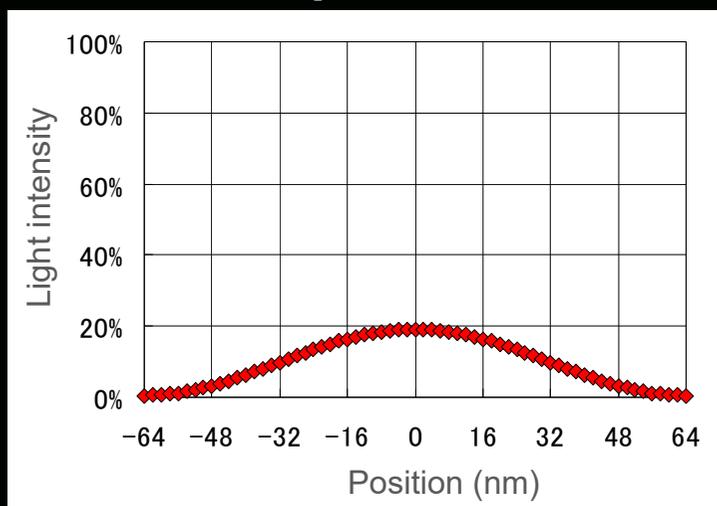
Resist materials development : “ Never Stop ”



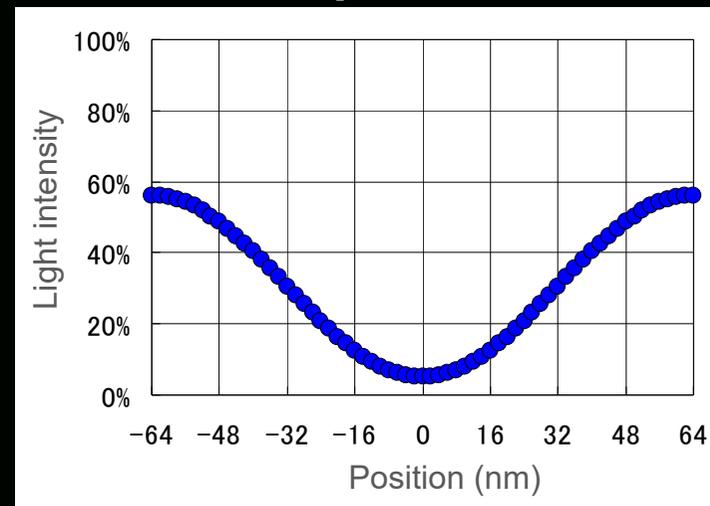
Theory of Optical Contrast Utilization (PTI vs NTI)



Prepare Trench pattern by PTI



Prepare Trench pattern by NTI

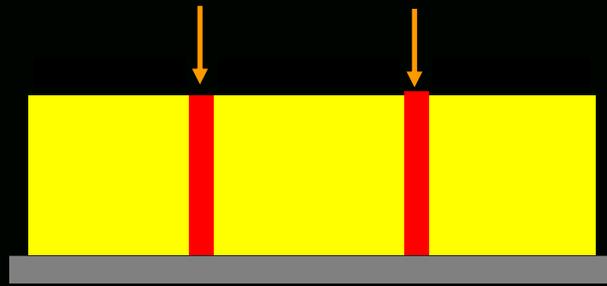


Trench pattern
32nm 1:3

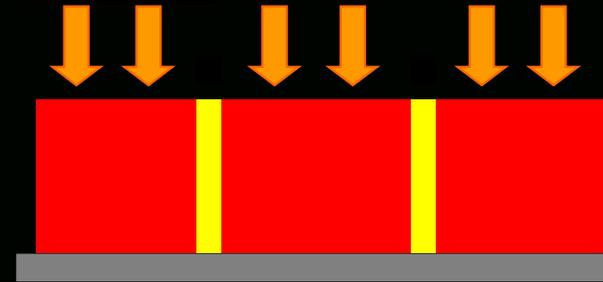
High resolution can be expected by strong contrast with NTI process.
Resist materials development : "Never Stop"



Theory of Optical Contrast Utilization (PTI vs NTI)



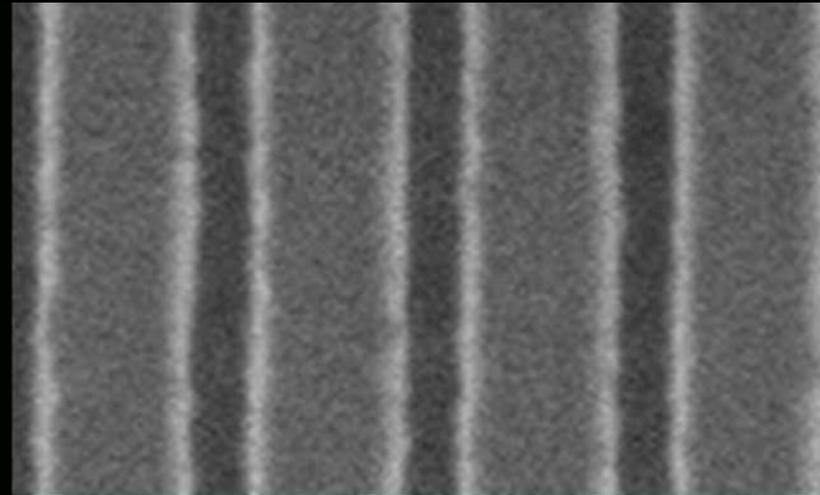
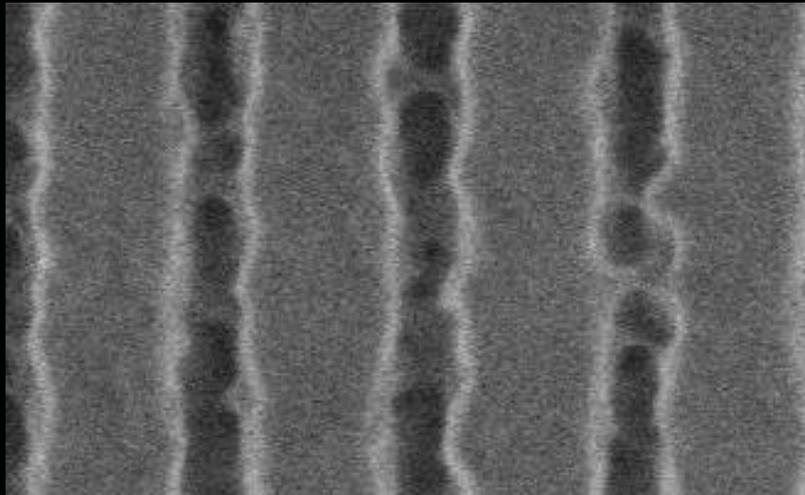
Prepare Trench pattern
by PTI



Prepare Trench pattern
by NTI

Trench pattern
32nm 1:3

NTI process observed brilliant resolution, useful for multiple patterning !!



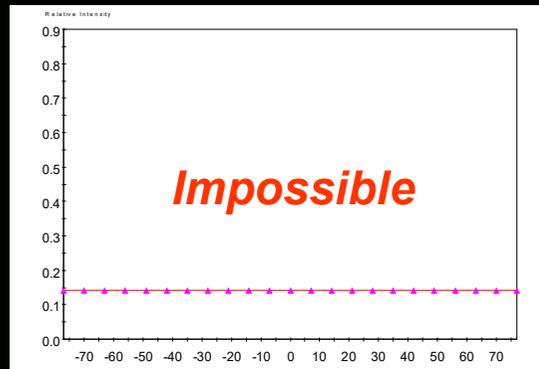
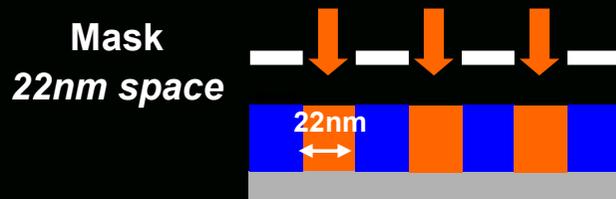
Resist materials development : “ Never Stop ”



What is NTI useful for ?

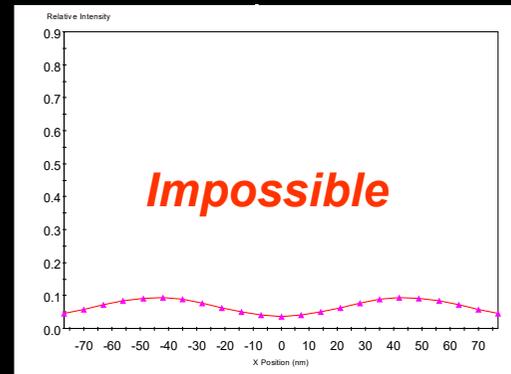
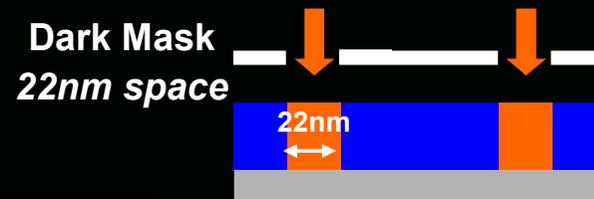
For realizing small CD patterning
Example) Prepare CD=22nm LS (1:1)

Single Patterning TCD=22nm



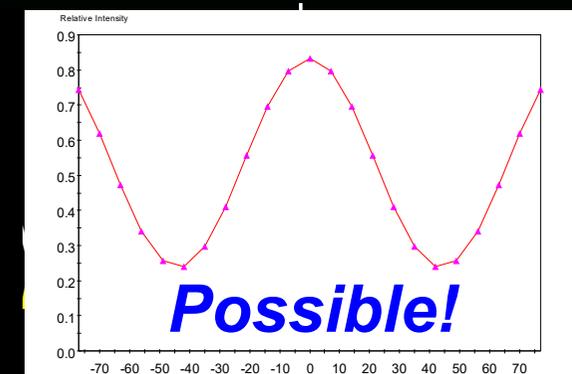
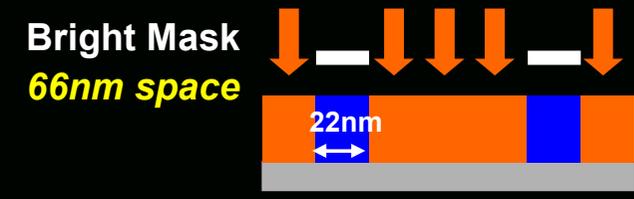
No light intensity

Double Patterning TCD=22nm with Positive-tone



Too low light intensity

Double Patterning TCD=22nm with Negative-tone



High light intensity !!

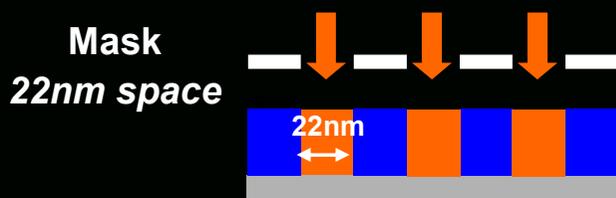
Resist materials development : " Never Stop "



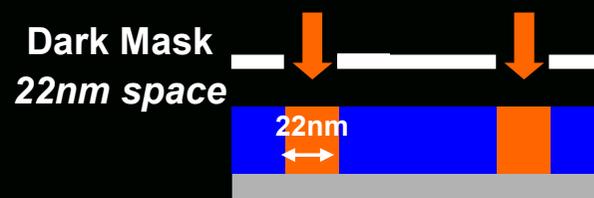
What is NTI useful for ?

For realizing small CD patterning
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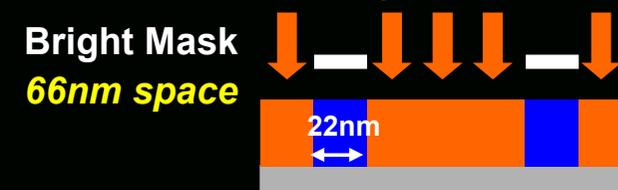
Single Patterning TCD=22nm



Double Patterning TCD=22nm with Positive-tone



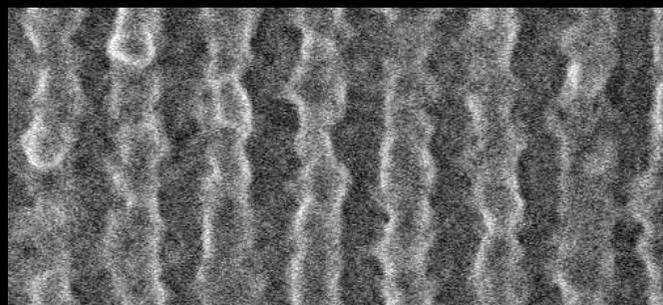
Double Patterning TCD=22nm with Negative-tone



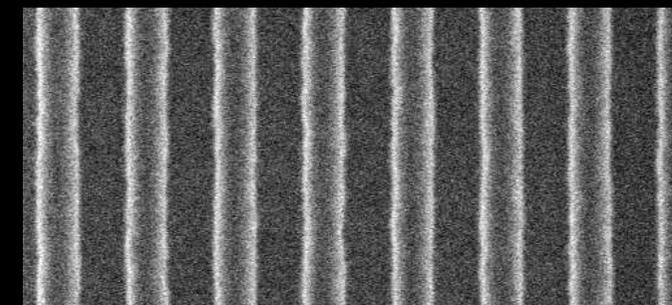
‘ Developer ’ : Very important !! Ultra pure solvent has to be used !!



No pattern



Patternable but ...



Brilliant pattern

Only double patterning with NTI can be observed brilliant pattern !!

Resist materials development : “ Never Stop ”



Advanced chips status

In 2018

Qualcomm
released SD 855 !



Impress Watch

7nm design rule

By using **ArF immersion** multi-patterning
without EUV lithography.

However, for next generation,
it necessary to use **EUV lithography**.

Is it true ?

More pattern shrinkage is needed ?

Possible to use EUV lithography for manufacturing ?

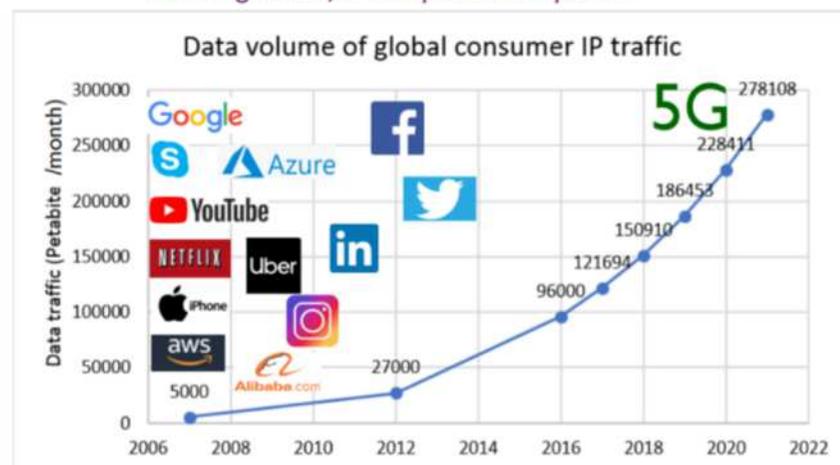
Resist materials development : “ Never Stop ”



Moore's low, still required ?

EXPONENTIAL INCREASE IN DATA VOLUME USAGE

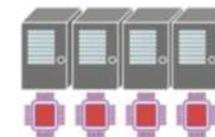
Growing need for computational power



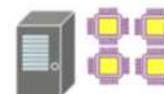
imec

INCREASE # TRANSISTORS IS STILL COST EFFECTIVE

1. Increase # Servers
(Scale out)



2. Increase # Chips
(Scale up)



3. Increase # Transistors
& Reduce data (Scale up)



Scaling

Machine learning



imec

Ryoung-Han Kim, imec, SPIE 2019

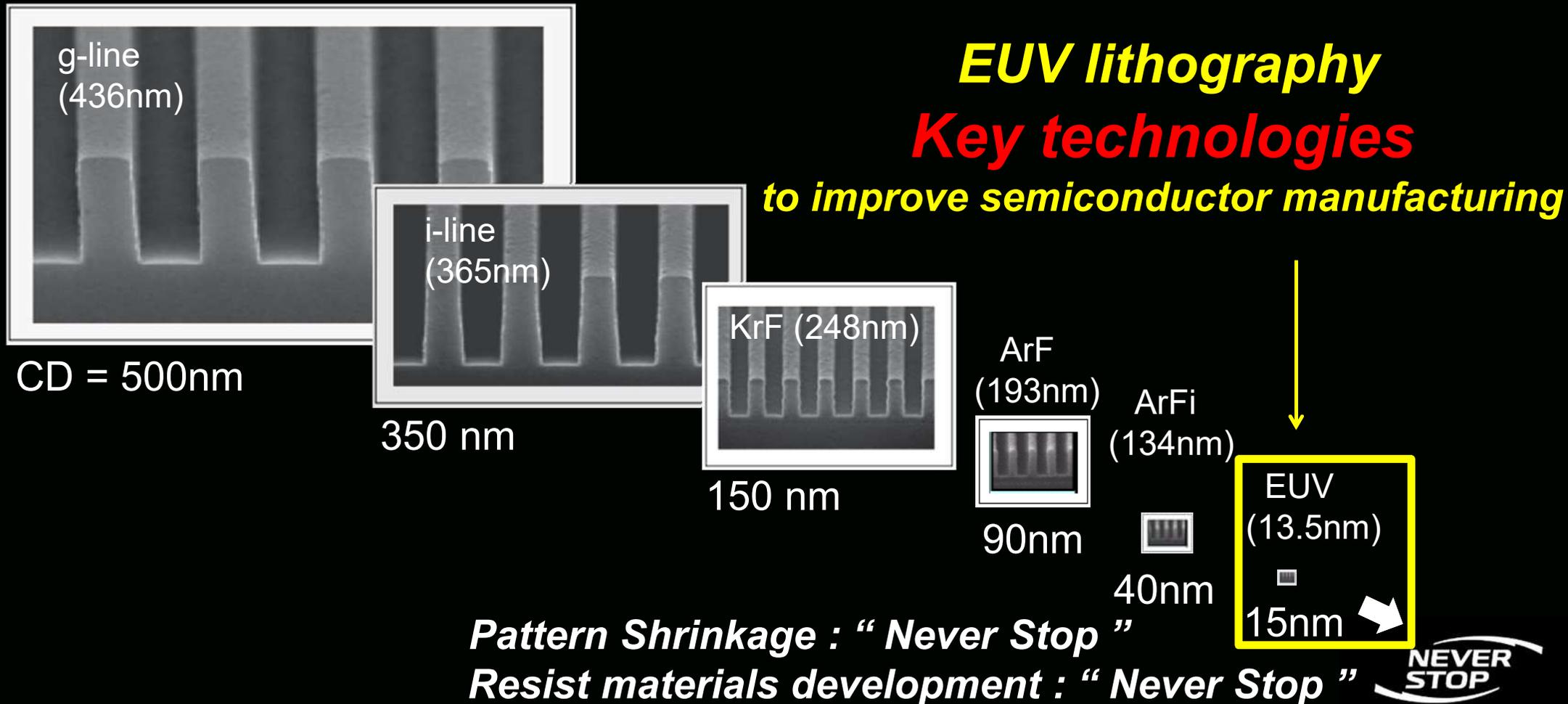
**Fortunately or unfortunately,
Still needed to follow and proceed 'Moore's low'.**

Resist materials development : " Never Stop "



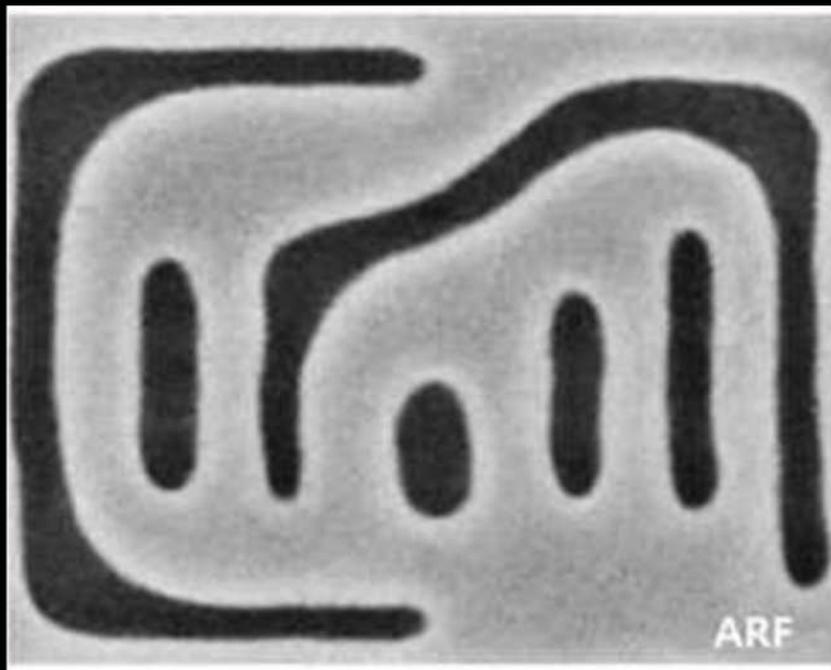
The Pattern shrinkage history

Pattern shrinkage has been driven by shorter exposure wavelength.

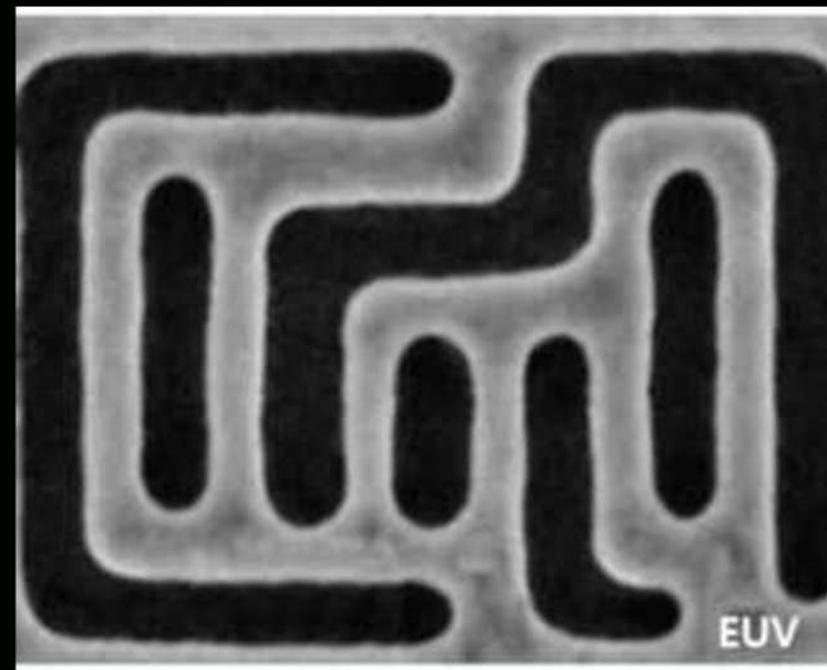


Why need EUV lithography ?

1st ; Pattern quality ; example



ArF i



EUV

Source: Samsung

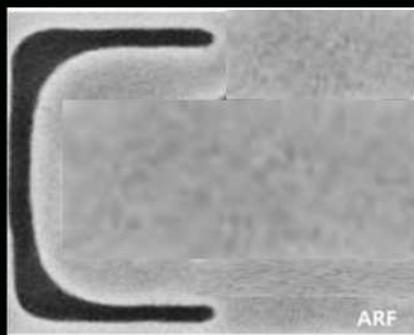
Resist materials development : “ Never Stop ”



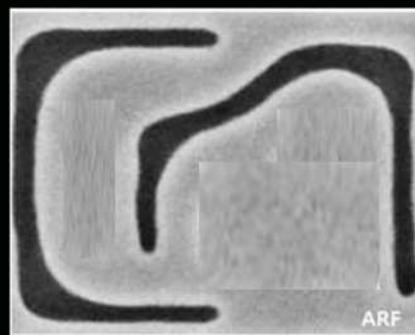
Why need EUV lithography ?

2nd ; Lithography steps ; example

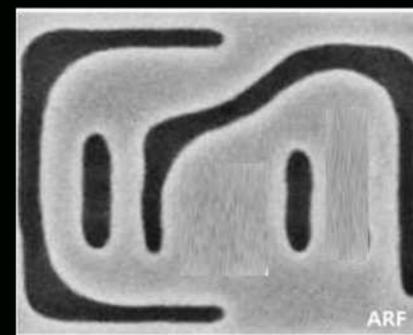
ArF i



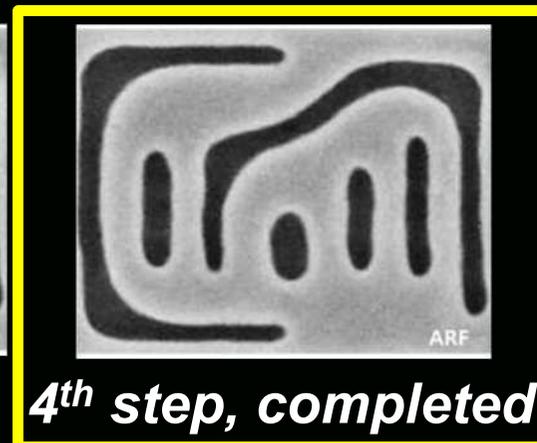
1st step



2nd step



3rd step



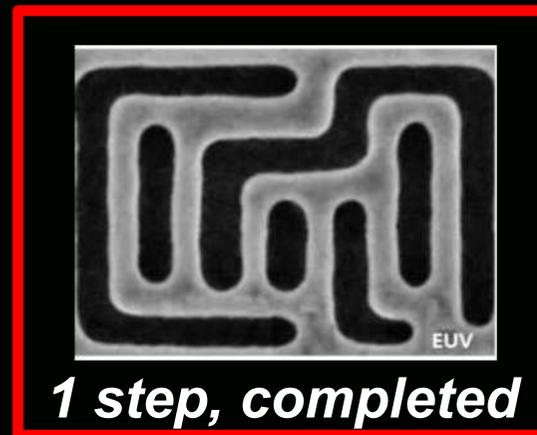
4th step, completed

Many steps and masks needed...

EUV



Only 1 step and 1 mask !!



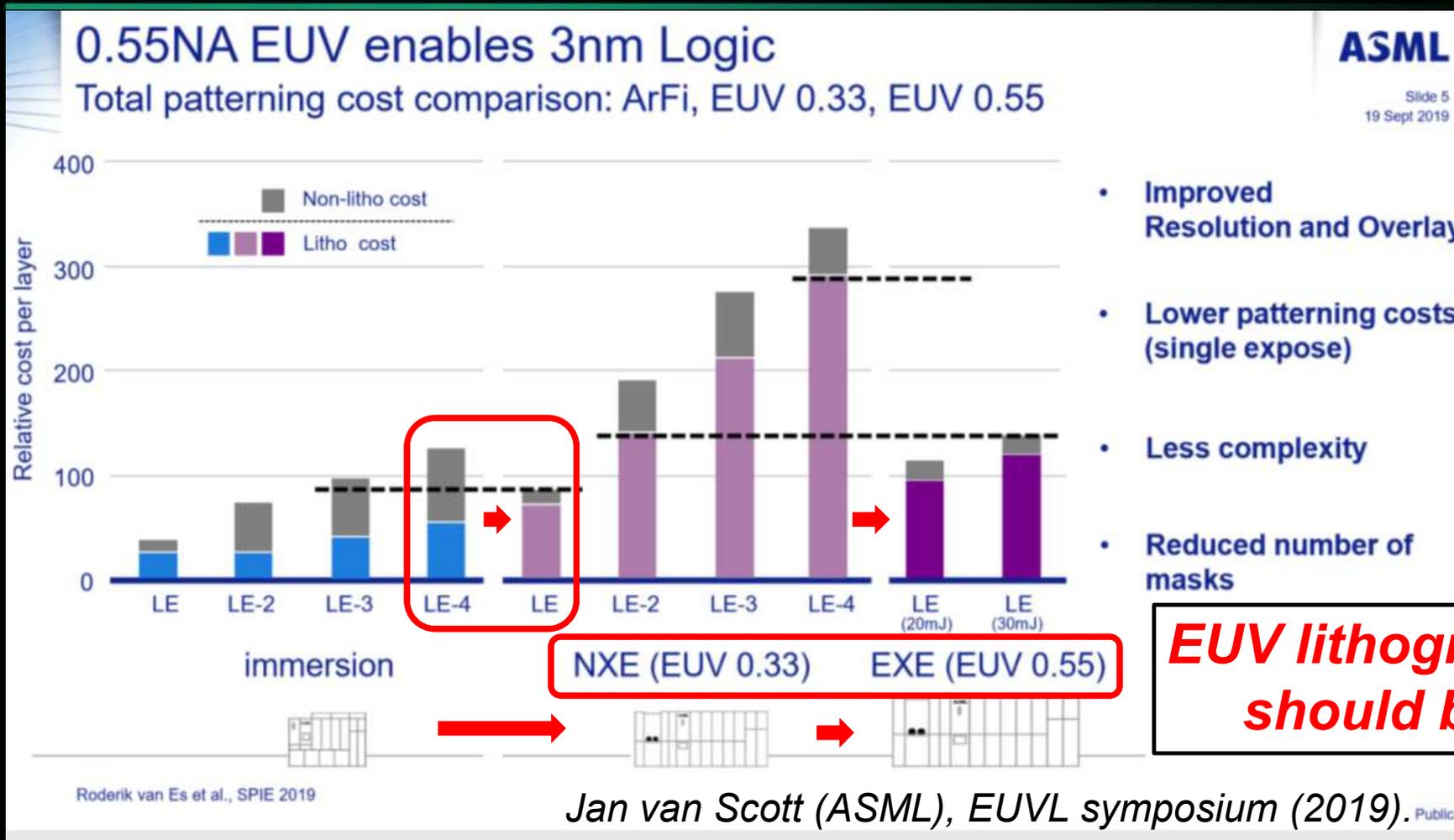
1 step, completed

Resist materials development : " Never Stop "



Source;
Pattern picture : Samsung
Lithography steps example : Prepared by author

Why need EUV lithography ?



- Improved Resolution and Overlay
- Lower patterning costs (single expose)
- Less complexity
- Reduced number of masks

Resist materials development : "Never Stop"



Recent advanced chips status

In 2019 (Reiwa 1 (令和 元年)) **Anniversary for EUV enthusiasts !**

Finally, EUV generation has come in 2019 !!

7nm+ design rule was applied to HVM by using EUV lithography !!

Qualcomm



Qualcomm
snapdragon

865

865 5G Mobile Platform

K-tai. watch. impress

HUAWEI Kirin 990 Series¹

Rethink Evolution

World's 1st Flagship 5G SoC powered with 7nm+ EUV²



Kirin 990
5G

HP; Huawei



SAMSUNG
Exynos
990

HP; Samsung



Already installed to
5G smart phone in 2020

Resist materials development : " Never Stop "



Recent advanced chips status

In 2020 **Already 5nm/5nm+ design rule ...**



Qualcomm HP



Samsung HP

An infographic for the Apple A14 chip. It features several icons and text boxes: "Machine learning controller" with an ML icon, "New 6-core CPU" with a CPU icon, "Next-generation ML accelerators" with a neural network icon, "16-core NEURAL ENGINE" with the text "NEURAL ENGINE", "5 nanometer process" in large blue text, "11.8 billion Transistors" in large white text, "Apple A14" with the Apple logo, "11 trillion Operations per second" in large blue text, "Advanced image signal processor" with a camera icon, "New 4-core GPU" with a GPU icon, and "Secure Enclave" with a lock icon.

Apple.com
News.mynavi.jp

Resist materials development : " Never Stop "



Recent advanced chips status

7nm/7nm+ design rule

5nm/5nm+ design rule

3nm design rule

2nm design rule

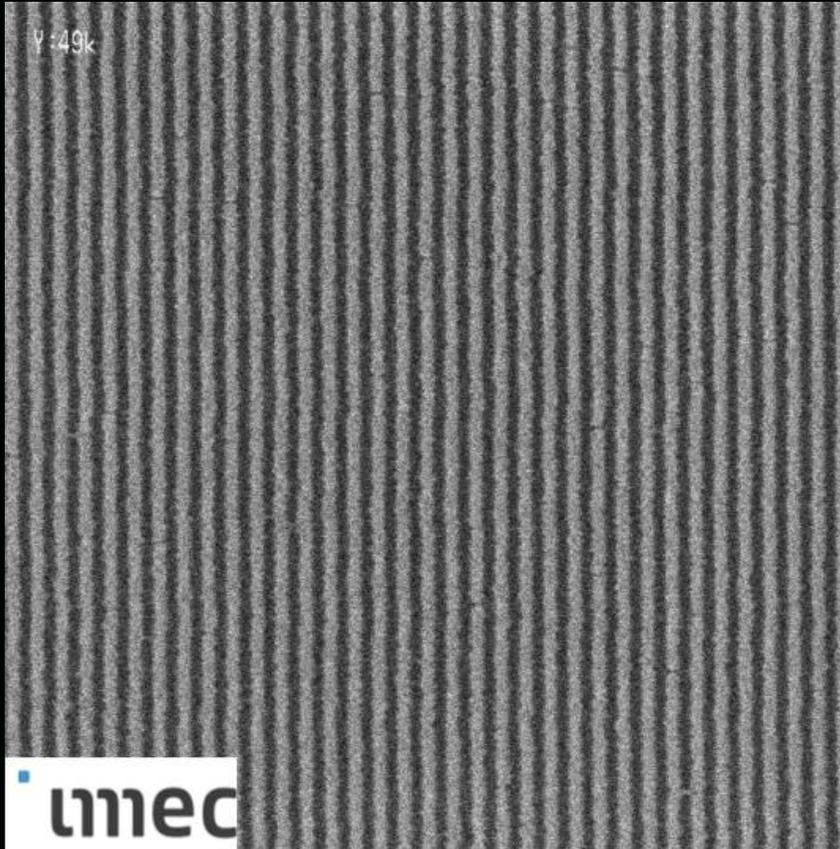
14A design rule

Pattern Shrinkage : “ Never Stop ”

Resist materials development : “ Never Stop ”



Challenging of EUV resist



HP13nm

$E_{opt} = 42 \text{ mJ/cm}^2$

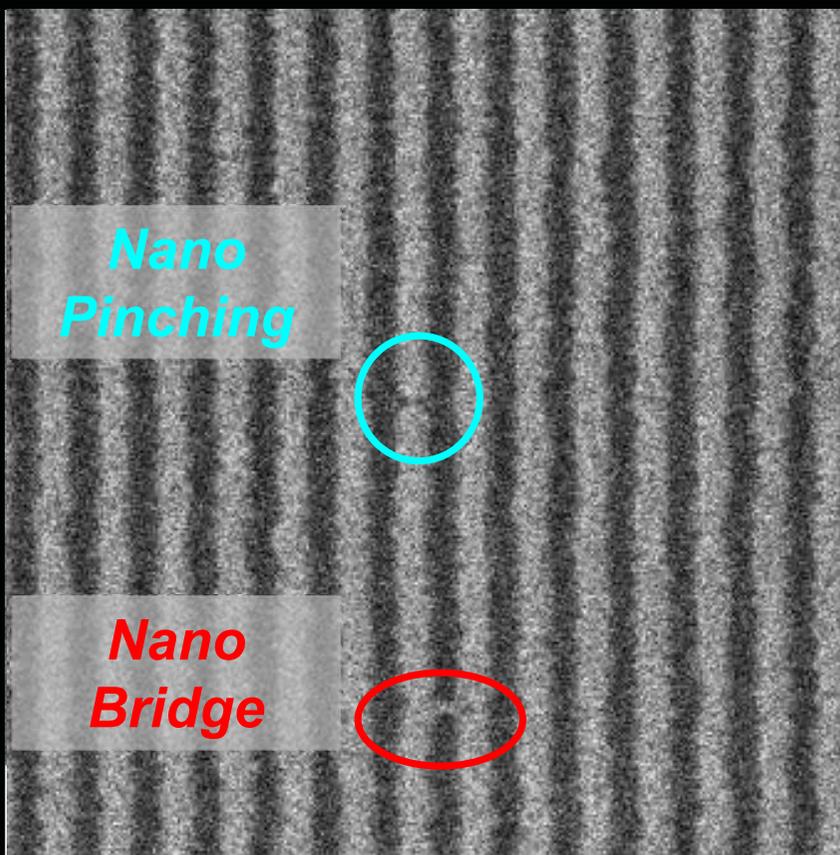
LWR = 5.3 nm

The resolution looks good enough.

Resist materials development : “ Never Stop ”



Challenging of EUV resist



HP13nm

$E_{opt} = 42 \text{ mJ/cm}^2$

LWR = 5.3 nm

The resolution looks good enough.

However, '**stochastic error**',
"Nano-Bridge" and **"Nano-Pinching"**
were observed.

=> Becomes an obstacle for HVM.

How to reduce 'stochastic error' ?

Resist materials development : "Never Stop"



Challenging of EUV resist

Have you ever heard “**stochastic**” ? Basically, it means...

What is the **stochastic** issues ?

Why now ?? No issues before ?

Random

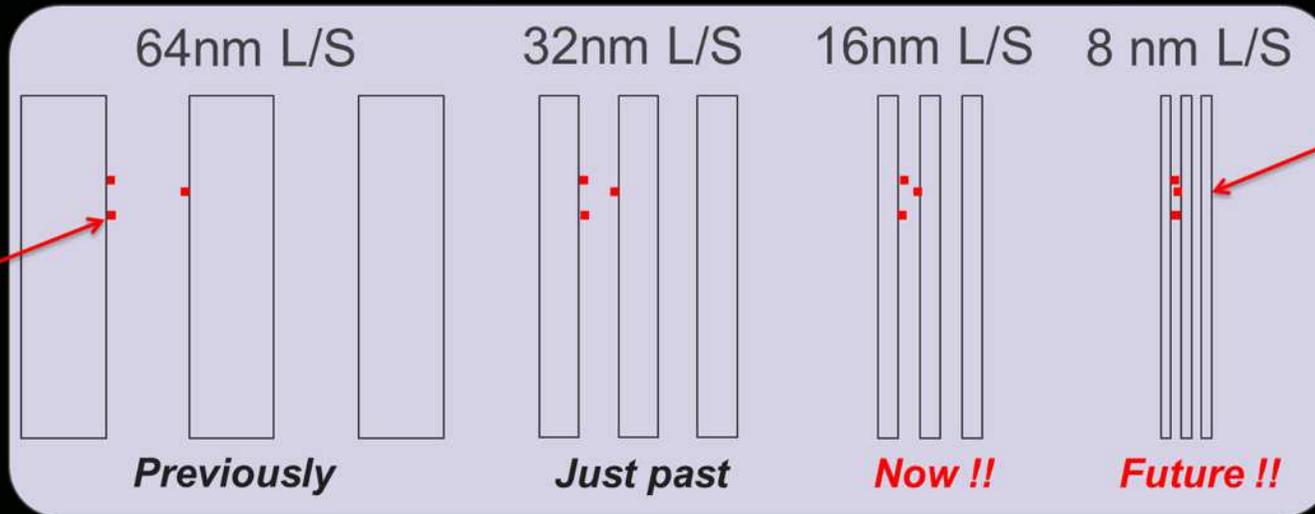
随机

隨機

Influence of pattern size shrinkage !

Let us imagine ;

No impact



Huge impact

Resist materials development : “ Never Stop ”



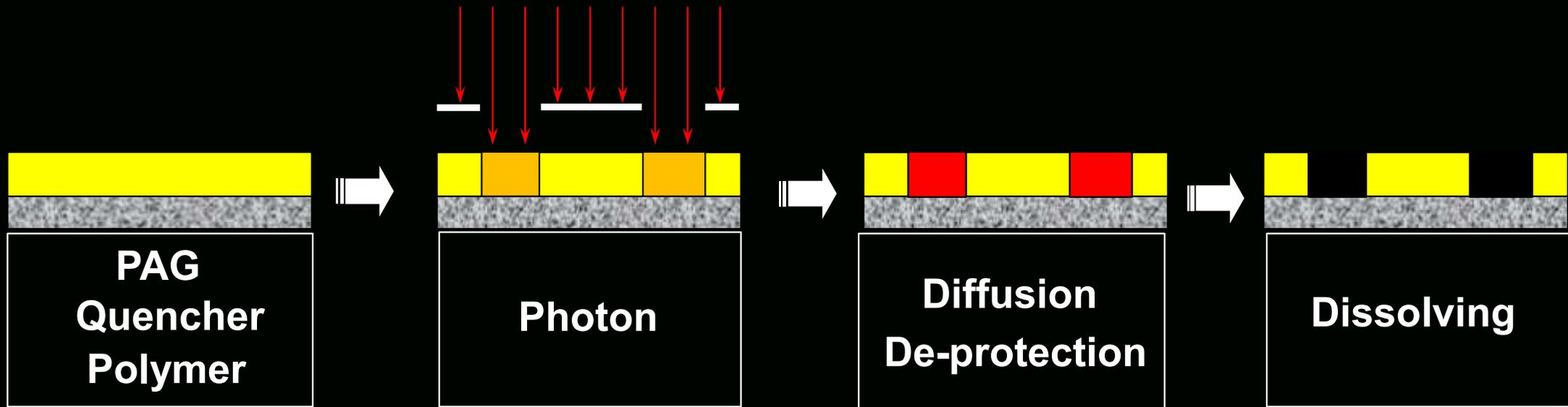
Stochastic factors in lithography

Resist coating

Exposure

*Post exposure
Bake*

Development



Materials location

**Poor photon number
Exposure locality**

**Location of
reaction points**

**Dissolving locality
Swelling behavior**

Resist materials development : " Never Stop "



1) Photon Stochastic

2) Chemical Stochastic

2)

Materials location

1)

Poor photon number
Exposure locality

2)

Location of
reaction points

2)

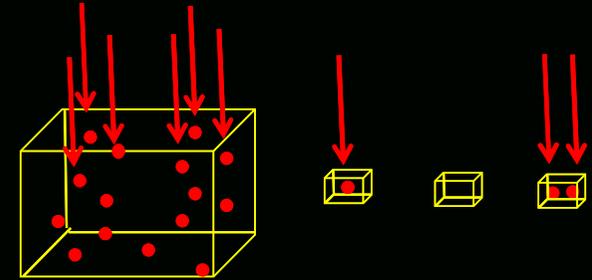
Dissolving locality
Swelling behavior

Resist materials development : “ Never Stop ”



How to reduce the stochastic factor ?

- 1) Photon Stochastic** (photon shot noise)
< Cause : light source > Poor photon number.



2) Chemical Stochastic

< Cause : resist materials and processes >

The materials location randomness, the reaction randomness in the film.

The dissolving randomness during the development process.

Resist materials development : “ Never Stop ”



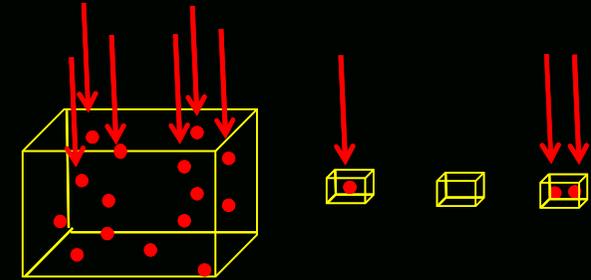
How to reduce the stochastic factor ?

1) **Photon Stochastic** (photon shot noise)

< Cause : light source > Poor photon number.

=> The resist materials can help it.

Introduce the function of 'catch more photon'.



2) **Chemical Stochastic**

< Cause : resist materials and processes >

The materials location randomness, the reaction randomness in the film.

=> **The functionalized materials are effective.**

The dissolving randomness during the development process.

=> **Organic solvent development is effective.**

Resist materials development : " Never Stop "



How to reduce the stochastic factor ?

2) Chemical Stochastic

< Cause : resist materials and processes >

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Resist materials development : “ Never Stop ”



How to reduce the stochastic factor ?

2) Chemical Stochastic

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The dissolving randomness during the development process.

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Resist materials development : “ Never Stop ”



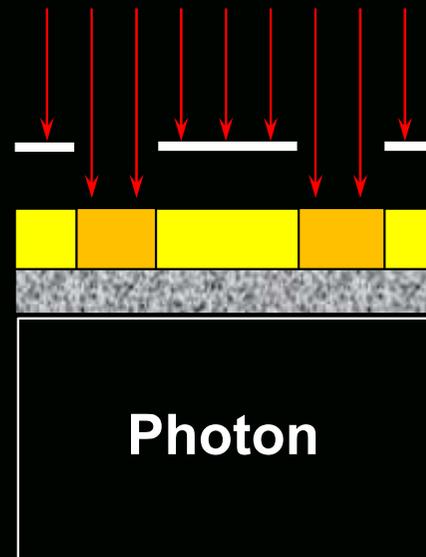
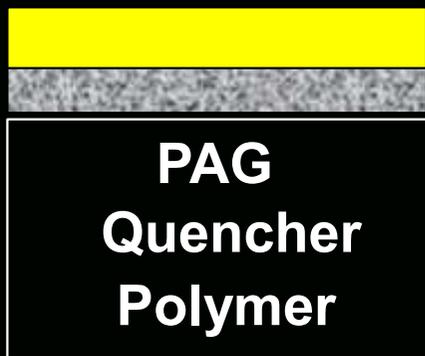
Stochastic factors in lithography

Resist coating

Exposure

*Post exposure
Bake*

Development



Materials location

**Poor photon number
Exposure locality**

**Location of
reaction points**

**Dissolving locality
Swelling behavior**

Resist materials development : " Never Stop "



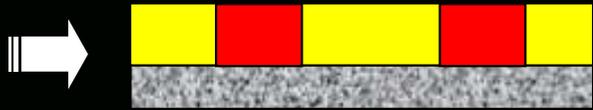
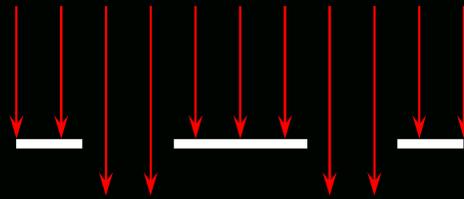
How to reduce the stochastic factor ? NTI process

Key point : Developer (Alkali aqueous based or Organic solvent based)

Resist coating



Exposure & Bake



Development

TMAH aq.



PTI (Positive Tone Imaging)

Organic Solvent



NTI (Negative Tone Imaging)

Negative Tone Imaging process is expected to reduce 'Chemical Stochastic'.

Organic compounds with organic solvent.
Dissolving smoothly ? Less Swelling ?

Resist materials development : " Never Stop "



How to reduce the stochastic factor ? NTI process

In situ dissolving behavior evaluation by using High Speed AFM.

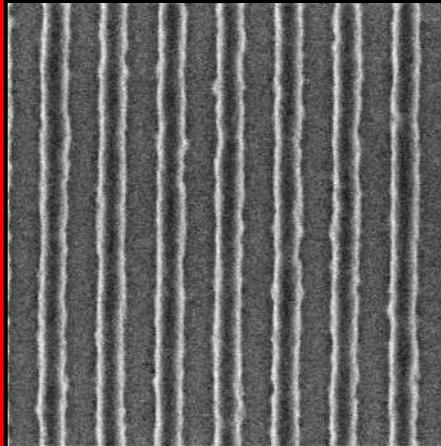
Development
time

Positive-tone

Negative-tone

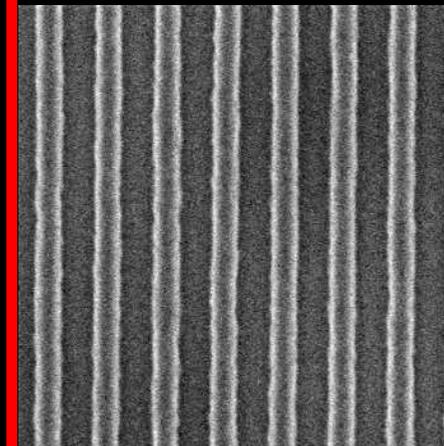
Negative-tone : extremely better LWR

14.8 mJ
LWR=4.8nm



Exposed with SFET

14.8 mJ
LWR=3.0nm



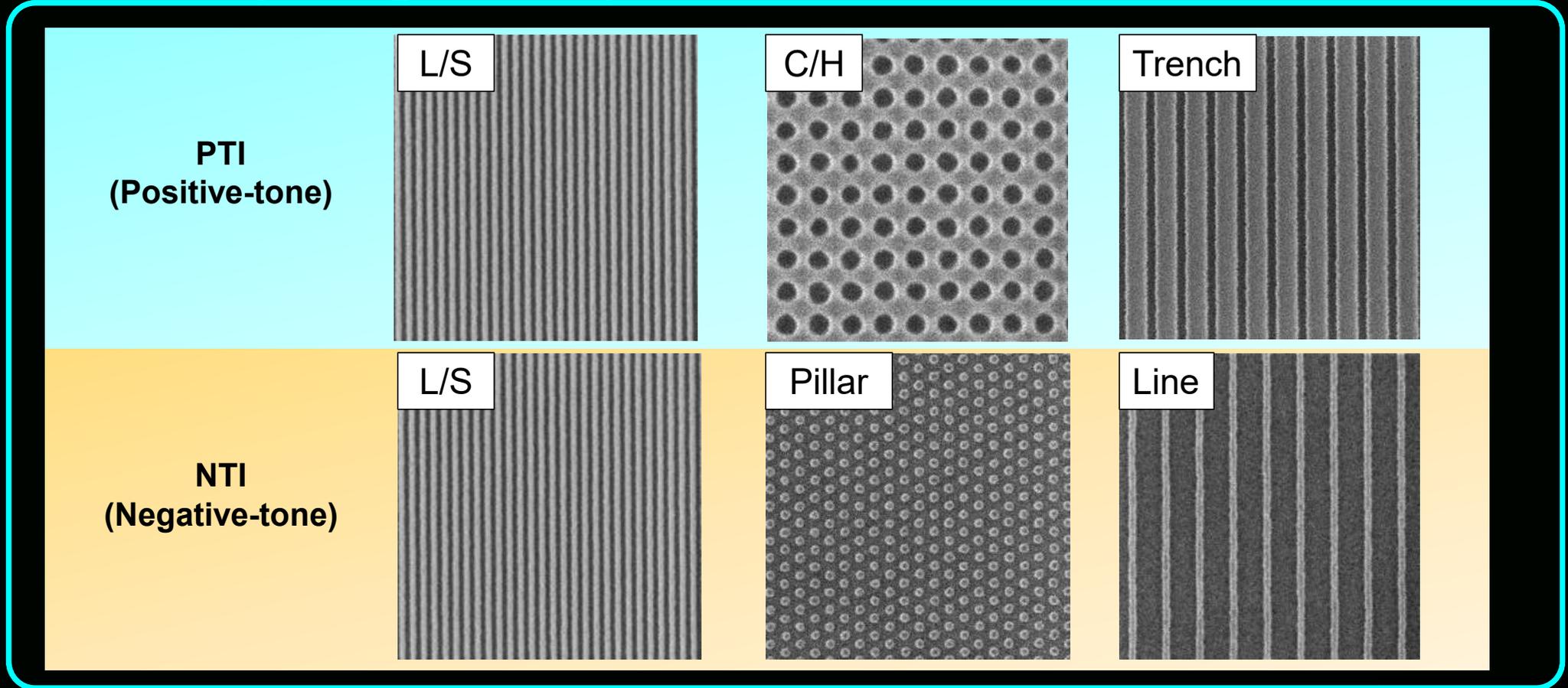
Exposed with SFET

Resist materials development : “ Never Stop ”



Summary

Excellent improving the litho performance due to reduce the stochastic issue.



Resist materials development : “ Never Stop ”



Summary

Negative-tone imaging, NTI, using organic solvent developer, showed excellent improving the lithographic performance both ArF immersion lithography and EUV lithography.

**ArF immersion ; With multiple-patterning,
successfully patternable for 10 / 7 nm and beyond**

EUV ; successfully reduced 'Chemical Stochastic' issue.

=> Expected to apply the real EUV lithography generation !!



If you have any questions, comments, or would like to communicate with me, please let me know.

You can send me an e-mail.

toru.fujimori@fujifilm.com

Resist materials development : " Never Stop "



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